

**WHAT IS CLAIMED IS:**

1. A method of manufacturing a microelectronic device, comprising:

providing a substrate having a plurality of partially completed microelectronic devices including at least one partially completed memory device and at least one partially completed transistor;

protecting at least a portion of the partially completed transistor by forming a first layer over the portion of the partially completed transistor to be protected during a subsequent material removal step;

forming a second layer substantially covering the partially completed memory device and the partially completed transistor;

removing portions of the second layer, leaving a portion of the second layer over the partially completed memory device; and

removing at least a substantial portion of the first layer from the partially completed transistor after the portions of the second layer are removed.

2. The method of claim 1 wherein the partially completed memory device comprises a partially completed floating gate field effect transistor device.

3. The method of claim 1 wherein said partially completed transistor comprises a partially completed MOSFET.

4. The method of claim 1 wherein the plurality of partially completed microelectronic device includes at least one partially completed field effect transistor (FET).

5. The method of claim 1 wherein the first layer comprises a dielectric material having a dielectric constant ranging between about 5.5 and about 9.

6. The method of claim 1 wherein the portions of the second layer are removed by at least one of a chemical mechanical polishing ( CMP ) process and an etching process.

7. The method of claim 1 wherein the first layer comprises an oxygen containing layer.
8. The method of claim 1 wherein the first layer comprises a nitride containing layer.
9. The method of claim 1 wherein the second layer comprises a gate electrode layer.
10. The method of claim 9 wherein the gate electrode layer has a thickness ranging between about 300 angstroms and about 2000 angstroms.
11. The method of claim 9 wherein the gate electrode layer comprises a silicon containing layer formed by an LPCVD process.
12. The method of claim 1 wherein the second layer comprises a gate dielectric layer.
13. The method of claim 12 wherein the gate dielectric layer has a thickness ranging between about 10 angstroms and about 300 angstroms.
14. The method of claim 12 wherein the gate dielectric layer comprises an oxygen containing layer formed by a thermal process.
15. A method of manufacturing a microelectronic device, comprising:  
providing a substrate having a protective layer located thereon and a plurality of isolation structures extending through the protective layer and at least partially into the substrate;  
forming a mask over a first portion of a surface collectively formed by the protective layer and the plurality of isolation structures, the masked first portion thereby sharing a boundary with an unmasked second portion of the surface;  
removing sacrificial portions of the protective layer from within the unmasked second portion;  
removing the mask;

forming a conformal layer over remaining portions of the protective layer, the isolation structures, and in voids created by the removal of the sacrificial portions of the protective layer;

planarizing the conformal layer such that the conformal layer, the isolation structures, and the remaining portions of the protective layer are substantially coplanar;

removing the remaining portions of the protective layer; and

forming transistors in voids created by the removal of the remaining portions of the protective layer.

16. The method of claim 15 wherein planarized portions of the conformal layer located between opposing isolation structures at least partially form a memory device.

17. The method of claim 15 wherein the memory device is a floating gate field effect transistor device.

18. The method of claim 15 wherein the transistors formed in the voids include MOSFETs.

19. The method of claim 15 wherein the substrate is selected from the group consisting of:

a silicon containing substrate;

a silicon-on-insulator (SOI) substrate;

a germanium epitaxial layer on a silicon substrate;

a germanium epitaxial layer on a sapphire substrate;

a silicon on nothing ( SON ) substrate;

a plastic substrate; and

a flexible substrate.

20. The method of claim 15 wherein the protective layer comprises a dielectric material having a dielectric constant ranging between about 5.5 and about 9.

21. The method of claim 15 wherein the protective layer comprises a nitrogen containing layer.

22. The method of claim 15 wherein the protective layer comprises an oxygen containing layer.

23. The method of claim 15 wherein the conformal layer comprises a gate electrode layer.

24. The method of claim 23 wherein the gate electrode layer has a thickness ranging between about 300 angstroms and about 2000 angstroms.

25. The method of claim 23 wherein the gate electrode layer comprises a silicon containing layer formed by an LPCVD process.

26. The method of claim 15 wherein planarizing the conformal layer comprises planarizing by at least one of a chemical mechanical polishing ( CMP ) process and an etching process.

27. The method of claim 15 further comprising forming a recessed portion of the conformal layer after planarizing the conformal layer.

28. A method of manufacturing a microelectronic device, comprising:

providing a substrate having a protective layer located thereon and a plurality of isolation structures extending through the protective layer and at least partially into the substrate, the substrate including at least one memory cell region and at least one periphery region;

forming a mask over at least a portion of the periphery region and exposing at least a portion of the memory cell region;

removing sacrificial portions of the protective layer from within the memory cell region;  
removing the mask;

forming a conformal layer over remaining portions of the protective layer, the isolation structures, and in voids created by the removal of the sacrificial portions of the protective layer;

planarizing the conformal layer such that the conformal layer, the isolation structures, and the remaining portions of the protective layer are substantially coplanar;

removing the remaining portions of the protective layer; and

forming transistors in voids created by the removal of the remaining portions of the protective layer.

29. The method of claim 28 wherein the memory device is a floating gate field effect transistor device.

30. The method of claim 28 wherein the transistors formed in the voids include MOSFETs.

31. The method of claim 28 wherein the substrate is selected from the group consisting of:

a silicon containing substrate;

a silicon-on-insulator (SOI) substrate;

a germanium epitaxial layer on a silicon substrate;

a germanium epitaxial layer on a sapphire substrate;

a silicon on nothing ( SON ) substrate;

a plastic substrate; and

a flexible substrate.

32. The method of claim 28 wherein the protective layer comprises a dielectric material having a dielectric constant ranging between about 5.5 and about 9.

33. The method of claim 28 wherein the protective layer comprises a nitrogen containing layer.

34. The method of claim 28 wherein the protective layer comprises an oxygen containing layer.

35. The method of claim 28 wherein the conformal layer comprises a gate electrode layer.

36. The method of claim 35 wherein the gate electrode layer has a thickness ranging between about 300 angstroms and about 2000 angstroms.

37. The method of claim 28 wherein the gate electrode layer comprises a silicon containing layer formed by a LPCVD process.

38. The method of claim 28 wherein planarizing the conformal layer comprises planarizing by at least one of a chemical mechanical polishing ( CMP ) process and an etching process.

39. The method of claim 28 further comprising forming a recessed portion of the conformal layer after planarizing the conformal layer.

40. An integrated circuit device, comprising:

a substrate having at least one memory cell region and at least one periphery region;

a plurality of isolation structures located in the memory cell region;

a plurality of active regions each located between proximate ones of the plurality of isolation structures;

a plurality of gate electrode layers each located between ones of the plurality of isolation structures and overlying a corresponding one of the plurality of active regions, each of the plurality of gate electrode layers having a width greater than a separation distance of adjacent ones of the plurality of isolation structures contacted by the corresponding gate electrode layer.

41. The integrated circuit device of claim 40 wherein each of the plurality of gate electrodes includes a portion extending into an adjacent one of the plurality of isolation structures.

42. The integrated circuit device of claim 40 wherein each of the plurality of gate electrode layers includes a side surface contacting an adjacent one of the plurality of isolation structures.

43. The integrated circuit device of claim 40 wherein each of the plurality of gate electrode layers overhangs a corresponding one of the plurality of active regions.

44. The integrated circuit device of claim 40 wherein each of the plurality of isolation structures includes a concave divot having a profile corresponding to a convex profile of an end of an adjacent one of the plurality of gate electrode layers.

45. The integrated circuit device of claim 40 wherein each of the plurality of isolation structures extends above the substrate at least to a height of adjacent ones of the plurality of gate electrode layers over the substrate.

46. The integrated circuit device of claim 40 wherein each of the plurality of isolation structures extends substantially beyond adjacent ones of the plurality of gate electrode layers in a direction away from the substrate.

47. The integrated circuit device of claim 40 wherein each of the plurality of gate electrode layers extends no further away from the substrate than adjacent ones of the plurality of isolation structures.

48. The integrated circuit device of claim 40 wherein each of the plurality of further comprising a plurality of logic circuitry transistors located in the periphery region.